

MC8051

Key Features

- Fully synchronous design
- Technology independent, clear structured, well commented VHDL source code
- Easily expandable by adapting/changing VHDL source code
- Parametrizeable design by simply changing VHDL constants
- User selectable number (N) of timers/counters and serial interface units
- Active timer/counter and serial interface units selected by additional special function register
- Instruction set compatible to the industry standard 8051 microcontroller
- Up to 10 times faster due to completely new architecture
- Optional implementation of the multiply command (MUL) using a parallel multiplier
- Optional implementation of the divide command (DIV) using a parallel divider
- Optional implementation of the decimal adjustment command (DA)
- No multiplexed I/O ports
- 256 bytes internal RAM
- Up to 64 kbyte ROM, up to 64 kbyte RAM
- Source code available free of charge under the GNU LGPL license

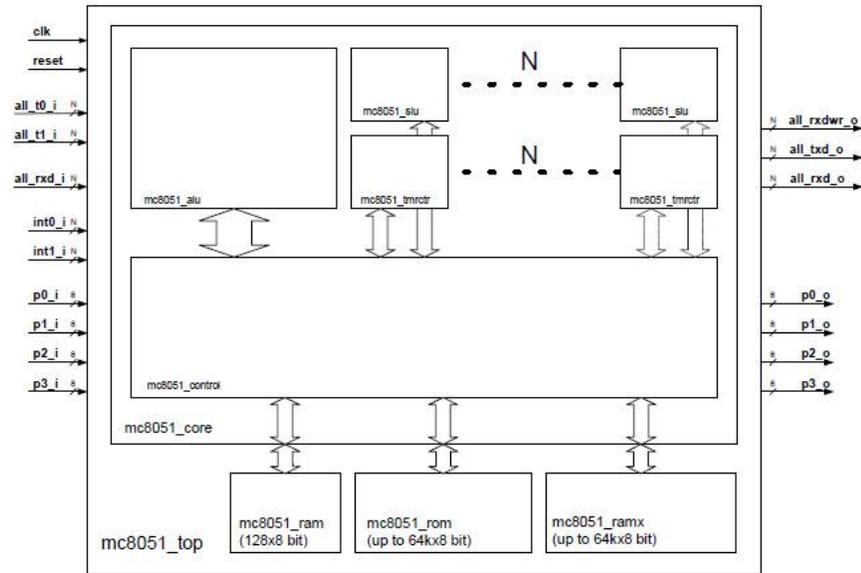


Fig 1. Block diagram: 8051 microcontroller IP core

Block Diagram

The starting from the top level module and its submodules are depicted in figure 1.

The toplevel signal names are shown as well as the three memory blocks used in the design. The user selectable number of serial interfaces and timer/counter units is indicated by the dotted line between the modules *mc8051_siu* and *mc8051_tmrcr*.

Clock Domains

The 8051 IP core is a fully synchronous design. There is a single clock signal that controls the clock input of every storage element. Clock gating is not used. The clock signal is not fed into any combinatorial element. The interrupt input lines are synchronized to the global clock signal using a standard two-level synchronization stage because they may be driven by external circuitry that operates with another clock. The parallel port input signals are not synchronized that way. If the user decides that there is also the need for synchronizing these signals it may be added easily.

Memory Interfaces

Due to the optimized architecture the signals coming from and going to the memory blocks have not been registered. So during synthesis input and output timing constraints should be placed on the corresponding ports and synchronous memory blocks should be used for the mc8051 IP-core.

Configuring the 8051 IP Core

In the following the parameterizability of the 8051 microcontroller IP-core design will be discussed and information for embedding the IP-core in larger designs will be given.

Timer/Counter, Serial Interface, and Interrupts

The original microcontroller design offered only 2 timer/counter units, one serial interface, and two external interrupt sources. 8051 derivatives later offered more of these resources on chip. Since this is sometimes a limiting factor we decided to implement some sort of parameterization in the 8051 IP core. This 8051 microcontroller IP-core offers the capability to generate up to 256 of these units by simply changing a VHDL constant's value. In the VHDL source file *mc8051_p.vhd* the constant *C_IMPL_N_TMR* can take values from 1 to 256 to control this feature. Values out of this interval result in a non-functioning configuration of the core.

Parallel I/O Ports

The mc8051 IP-core offers just as the original 8051 microcontroller 4 bidirectional 8bit I/O ports to conveniently exchange data with the microcontroller's environment. To ease integration of our core for IC design the original's multi-function ports have not been rebuilt and all signals (e.g. serial interface, interrupts, counter inputs, and interface to external memory) have been fed separately out of the core (see figure 1). The basic structure of the parallel I/O ports is shown in figure

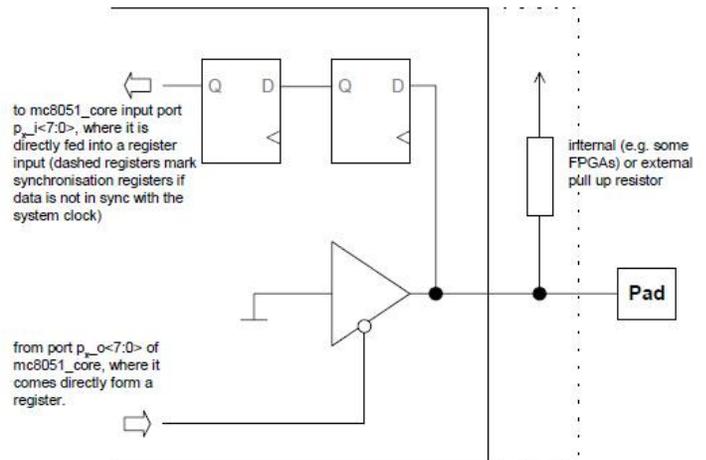


figure 6: Basic structure of the parallel I/O ports.