ADSP-2181

FEATURES

PERFORMANCE

25 ns Instruction Cycle Time from 20 MHz Crystal @ 5.0 Volts
40 MIPS Sustained Performance
Single-Cycle Instruction Execution
Single-Cycle Context Switch
3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
Multifunction Instructions
Power-Down Mode Featuring Low CMOS Standby
Power Dissipation with 100 Cycle Recovery from Power-Down Condition
Low Power Dissipation in Idle Mode

INTEGRATION

ADSP-2100 Family Code Compatible, with Instruction Set Extensions
80K Bytes of On-Chip RAM, Configured as
16K Words On-Chip Program Memory RAM
16K Words On-Chip Data Memory RAM
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides Zero Overhead Looping
Conditional Instruction Execution
Programmable 16-Bit Interval Timer with Prescaler
128-Lead TQFP/128-Lead PQFP

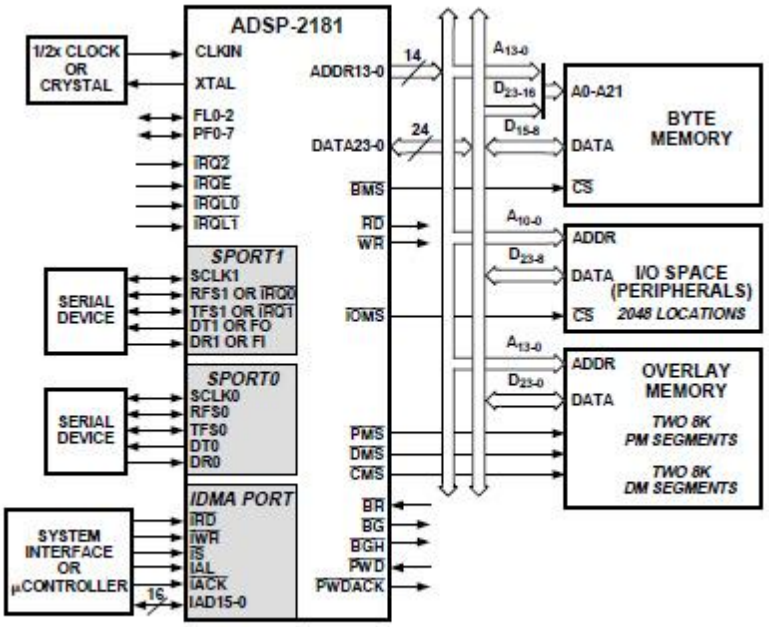

Figure 2. ADSP-2181 Basic System Configuration

SYSTEM INTERFACE

16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
4 MByte Memory Interface for Storage of Data Tables and Program Overlays
8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers
I/O Memory Interface with 2048 Locations Supports Parallel Peripherals
Programmable Memory Strobe and Separate I/O Memory Space Permits "Glueless" System Design
Programmable Wait State Generation
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
Six External Interrupts
13 Programmable Flag Pins Provide Flexible System Signaling
ICE-Port™ Emulator Interface Supports Debugging in Final Systems

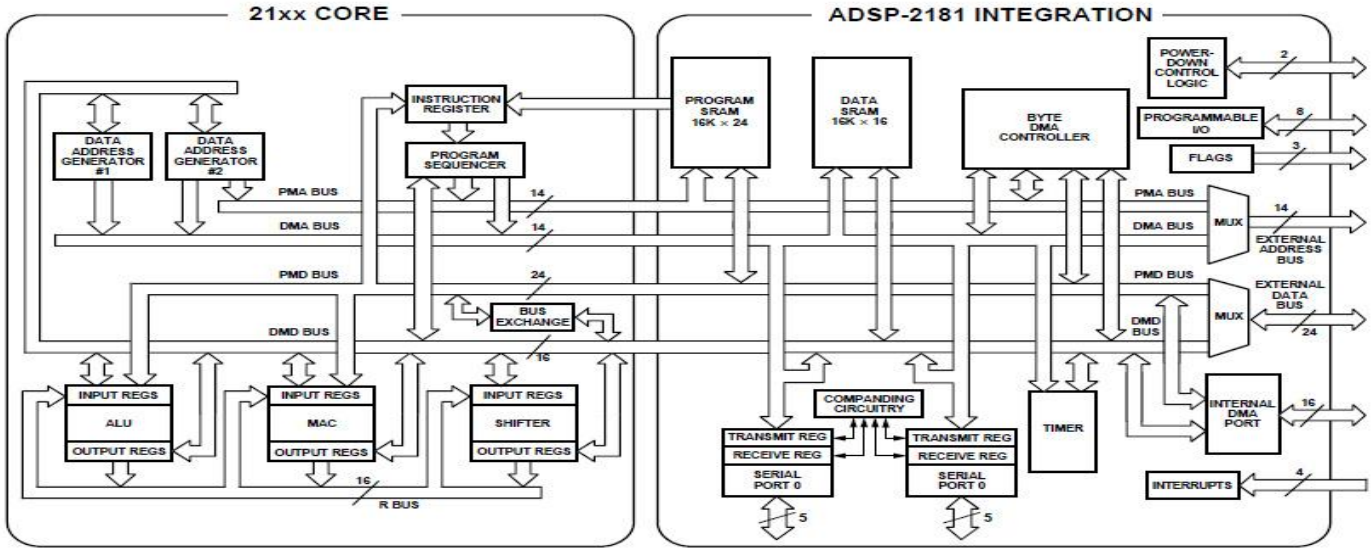

Figure 1. ADSP-2181 Block Diagram

The ADSP-2181 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications. The ADSP-2181 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2181 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2181 is available in 128-lead TQFP and 128- lead PQFP packages.

In addition, the ADSP-2181 supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test— new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers and global interrupt masking for increased flexibility.

Fabricated in a high speed, double metal, low power, CMOS process, the ADSP-2181 operates with a 25 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2181's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2181 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSP-2181 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2181 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development. Figure 1 is an overall block diagram of the ADSP-2181. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations. The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2181 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

• Program Memory Address (PMA) Bus
• Program Memory Data (PMD) Bus
• Data Memory Address (DMA) Bus
• Data Memory Data (DMD) Bus
• Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2181 to fetch two operands in a single cycle, one from program memory and one from data memory. TheADSP-2181 can fetch an operand from program memory and the next instruction in the same cycle.

In addition to the address and data bus for external memory connection, the ADSP-2181 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals (*BR*, *BGH* and *BG*). One execution mode (Go Mode) allows the ADSP-2181 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2181 can respond to 13 possible interrupts, eleven of which are accessible at any given time. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master *RESET* signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.
Each port can generate an internal programmable serial clock or accept an external serial clock.
The ADSP-2181 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs and three flags that are always outputs.
A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2181 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.
Here is a brief list of the capabilities of the ADSP-2181 SPORTs. Refer to the *ADSP-2100 Family User's Manual, Third Edition* for further details.

- SPORTs are bidirectional and have a separate, double buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and m-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (*IRQ0* and *IRQ1*) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Descriptions

The ADSP-2181 is available in 128-lead TQFP and 128-lead PQFP packages.

PIN FUNCTION DESCRIPTIONS

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Pin Name(s)	# of Pins	Input/ Output	Function
Address	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
Data	24	I/O	Data I/O Pins for Program and Data Memory Spaces (8 MSBs Are Also Used as Byte Space Addresses)
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{IRQ2}}$	1	I	Edge- or Level-Sensitive Interrupt Request
$\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$	2	I	Level-Sensitive Interrupt Requests
$\overline{\text{IRQE}}$	1	I	Edge-Sensitive Interrupt Request
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{IOMS}}$	1	O	I/O Space Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
MMAP	1	I	Memory Map Select Input
BMODE	1	I	Boot Option Control Input
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port 1 *or* Two External $\overline{\text{IRQ}}$s, Flag In and Flag Out
$\overline{\text{IRD}}$, $\overline{\text{IWR}}$	2	I	IDMA Port Read/Write Inputs
$\overline{\text{IS}}$	1	I	IDMA Port Select
IAL	1	I	IDMA Port Address Latch Enable
IAD	16	I/O	IDMA Port Address/Data Bus
$\overline{\text{IACK}}$	1	O	IDMA Port Access Ready Acknowledge
$\overline{\text{PWD}}$	1	I	Power-Down Control
PWDACK	1	O	Power-Down Control
FL0, FL1, FL2	3	O	Output Flags
PF7:0	8	I/O	Programmable I/O Pins
EE	1	*	(Emulator Only*)
$\overline{\text{EBR}}$	1	*	(Emulator Only*)
$\overline{\text{EBG}}$	1	*	(Emulator Only*)
$\overline{\text{ERESET}}$	1	*	(Emulator Only*)
$\overline{\text{EMS}}$	1	*	(Emulator Only*)
$\overline{\text{EINT}}$	1	*	(Emulator Only*)
ECLK	1	*	(Emulator Only*)
ELIN	1	*	(Emulator Only*)
ELOUT	1	*	(Emulator Only*)
GND	11	–	Ground Pins
VDD	6	–	Power Supply Pins